Electronic Version
Stylesheet Version v1.1.1

# Claims

[c1] What is claimed is:

1. A method for manufacturing a read only memory (ROM) device capable of shortening product turn-around time, the method comprising the steps of:

providing a semiconductor substrate having thereon an array of metal-oxide-semiconductor field-effect transistors (MOSFETs) within a ROM region and a dielectric layer covering the MOSFETs within the ROM region, wherein each of the MOSFETs has a gate, a source, and a drain, and wherein all of the MOSFETs are initially in an "ON" state;

forming a coding photoresist layer on the dielectric layer;

patterning the coding photoresist layer to form a plurality of apertures defining exposure windows where the underlying MOSFETs are to be coded from the "ON" state into an "OFF" state, wherein the exposure windows are disposed above the sources of the MOSFETs to be coded;

using the patterning coding photoresist layer as an etching hard mask to etch the dielectric layer, the sources of the MOSFETs to be coded, and a portion of the semiconductor substrate underneath the sources of the MOSFETs to be coded through the exposure windows to a depth

that is lower than a junction depth of the sources of the MOSFETs to be coded to form a deep trench, which disconnects the sources of the MOSFETs to be coded from source lines;
stripping the coding photoresist layer; and
depositing a gap fill layer over the dielectric layer to fill the deep trench.

[c2] 2. The method of claim 1 wherein each exposure window has a window length that is greater than a width of the source.

[c3] 3. The method of claim 1 wherein the dielectric layer has a thickness of between 2000 and 7000 angstroms.

[c4] 4. The method of claim 1 wherein after depositing a gap fill layer over the dielectric layer, the method further comprises:
forming contacts in the gap fill layer and the dielectric layer; and
forming bit lines over the gap fill layer within the ROM region.

[c5] 5. A method for manufacturing a read only memory (ROM) device capable of shortening product turn-around time, the method comprising:
providing a semiconductor substrate having thereon an

array of field-effect transistors within a ROM region and a first dielectric layer covering the array of field-effect transistors, wherein each of the MOSFETs has a gate, a drain, and a source connected to a source line, and wherein all of the field-effect transistors are initially in an "ON" state;

forming bit lines on the first dielectric layer within the ROM region, wherein the bit lines are covered by a second dielectric layer, and wherein the bit lines bypass the underlying sources of the array of the field-effect transistors to not overlap with the sources;

forming a coding photoresist layer on the second dielectric layer;

patterning the coding photoresist layer to form a plurality of apertures defining exposure windows where the underlying field-effect transistors are to be coded permanently to an "OFF" state;

implementing a code etching back process, using the patterned coding photoresist layer as an etching hard mask to etch the second dielectric layer, the first dielectric layer, the sources of the MOSFETs to be coded, and a portion of the semiconductor substrate underneath the sources of the MOSFETs to be coded through the exposure windows to a depth that is lower than a junction depth of the sources of the MOSFETs to be codedto form a deep trench that disconnects the sources of the MOS-

FETs to be coded from the source lines; and
stripping the coding photoresist layer.

[c6] 6. The method of claim 5 wherein after stripping the coding photoresist layer, the method further comprises: depositing a gap fill layer over the second dielectric layer to fill the deep trench.

[c7] 7. The method of claim 5 wherein a passivation layer is formed on the second dielectric layer.

[c8] 8. The method of claim 5 wherein each exposure window has a window length that is greater than a width of the source.